20.3 An Attachable Wireless Chip Access Interface for Arbitrary Data Rate Using Pulse-Based Inductive-Coupling through LSI Package

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Inductive coupling techniques have been widely used for proximity and short-range communications. The conventional inductive-coupling technique uses a LC resonator tuned to its carrier and only supports a data rate of several hundred kb/s associated with the carrier frequency. By contrast, pulse-based inductive-coupling communication uses no carrier, which brings advantages of adaptability to an arbitrary data rate of up to several Gb/s, as well as a simple transceiver architecture. Its application to short-range (several tens of μm) wideband wireless inter-chip connection for System-in-a-Package integration has been intensively studied [1,2]. If the communication distance is extended to the millimeter range, the pulse-based inductive-coupling technique opens up various new applications such as wireless on-chip bus tracking for debugging, package-on-package communications, wireless connectors, and high-speed non-contact memory access.

A high-speed wireless logic probing system is presented as one of the applications of the millimeter range carrierless inductive-coupling technique. A pulse transceiver for a wireless probe and its target LSI are fabricated using a 0.25μm standard CMOS logic process. A maximum data rate of 20Mb/s and a communication range of 1.2mm is achieved.

Figure 20.3.1 shows a configuration of the wireless logic probing system. The wireless probe consists of inductors that are patterned on a Flexible-Circuit-Board (FCB) and a probe IC. The combination of the FCB inductors and the probe IC is cost-effective, because the inductor pattern can be optimally customized according to the target LSI, whereas the probe IC can be designed for general use. The wireless probe can be controlled by a PC via an In-Circuit-Emulator (ICE) with a USB2.0 interface. In this study, an MCU chip housed in a 1mm thick SSOP package was chosen as the target LSI. The target LSI also contains a pulse transceiver with on-chip inductors formed by the top metal layer.

Figure 20.3.2 shows a block diagram of the pulse-based transceiver. An asynchronous channel for clock link and synchronous channels for full-duplex data up/down links can be established. A system clock for the target LSI is transmitted to the wireless probe, recovered by a hysteresis comparator, and then used for data synchronization in the probe IC. The hysteresis level can be controlled by changing the bias current of a latch (Fig. 20.3.3). A bi-phase modulation scheme [1,2] is adopted in the data link. The clock skew between the transmitter and the receiver is adjusted by a controllable delay line. Since both the target LSI and the probe IC use the same clock edge, the transmitted data can be robustly recovered even if the system clock has large jitter. An arbitrary data rate and system clock frequency can be chosen, which provides great flexibility to the system design.

Since the clock receiver uses an asynchronous comparator, ringing in the received signal or digital switching noise can cause glitches in the recovered clock. All such problems usually occur just after the clock edge. They can be avoided by introducing a de-glitching circuit (Fig. 20.3.3). An edge detector detects the rising and falling edges of the recovered clock and generates a short pulse. Using the short pulse as a trigger, a pulse expander generates a mask signal of several nano-seconds whose time constant can be determined by a current source and a MOS capacitor. During the time the mask signal is high, the latched value is held and glitches can be avoided. For further reliable communications, the up/down data links can be used for error detection by loop-back verification.

In pulse-based inductive-coupling communication, tradeoffs between the communication range and the data rate should be considered. The communication range can be extended by increasing the inductor size. The larger inductor, however, requires a longer pulse, because the larger inductor has a lower self-resonant frequency. Since the maximum attainable data rate is in inverse proportion to the pulse width, the larger inductor has a lower data rate. Furthermore, the probing system should have high alignment tolerance for easy handling. In this study, the inductors in the FCB and the target LSI are 1.0mm^2 and 0.6mm^2, respectively. The self-resonant frequency is 2GHz. Taking this into account, the pulse width is set to 1ns.

To extend the communication range under the size limitation of the inductor, received signals are amplified by 30dB using a 2-stage complementary differential amplifier prior to the comparator. DC offsets of the amplifier and the comparator cause a serious problem during signal detection. Though MIM capacitors have excellent frequency characteristics, they are not available here for use in DC-offset elimination, to maintain compatibility with standard CMOS processes. In this receiver, a 6b current steering DAC is used for the offset cancellation. During offset calibration, the transmitter is powered off and the comparator in the clock receiver operates without hysteresis. The DAC setting for the offset canceling can be determined by scanning the DAC input value and detecting the point where the polarity of the comparator output changes.

The waveform of the received signal in the data receiver can be traced using the DAC and clock delay line (Fig. 20.3.4). At fixed clock delay, the DAC input value is swept and the changing point of the comparator's output polarity is detected. The detected point corresponds to the received signal amplitude at the delay. The same procedure is repeated while the clock delay is swept. Since the transmitted pulse width is well controlled to avoid self-resonance, the received signal shows very small ringing. Although the required data rate is 20Mb/s in this system, Fig. 20.3.4 supports the fact that this wireless data link has a much higher potential data rate of up to 500Mb/s.

The Bit-Error Rate (BER) was measured as a function of the horizontal alignment error between the inductors in the target LSI and the FCB (Fig. 20.3.5). Using a spacer, the vertical communication distance is set at 1.2mm. From Fig. 20.3.5, the horizontal alignment tolerance is 0.5mm, which enables hand attachment.

A die micrograph is shown in Fig. 20.3.6. Die size is 9.4mm^2 including I/O buffers and bonding pads. The MCU core and the transceiver are designed using 2.5V MOSFETs, and the I/O buffers are designed using thick-oxide 5V MOSFETs. The chip contains two sets of transceivers. One set is used for the wireless logic probe with the FCB inductors. The other set is used for the target LSI with an on-chip inductor and MCU core. The active area of each transmitter is 0.006mm^2 and that of each receiver is 0.012mm^2. The chip features are summarized in Fig. 20.3.7.

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[2] N. Miura, et al., "A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link," *ISSCC Dig. Tech. Papers*, pp. 424-425, Feb., 2006.

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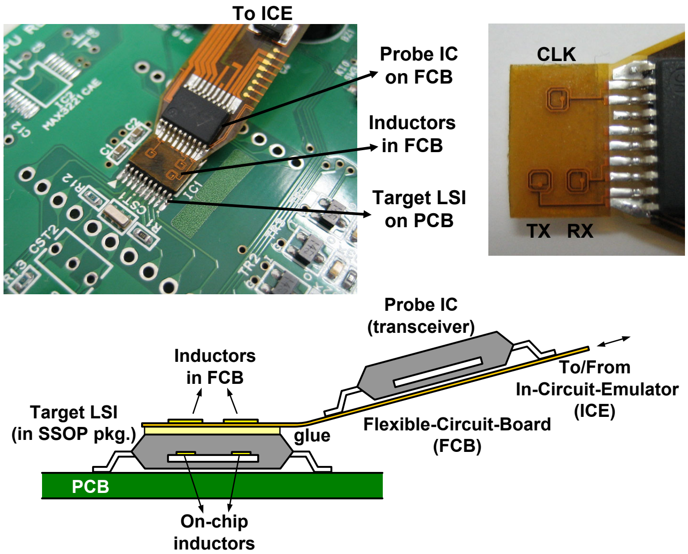

Figure 20.3.1: Wireless logic probing system.

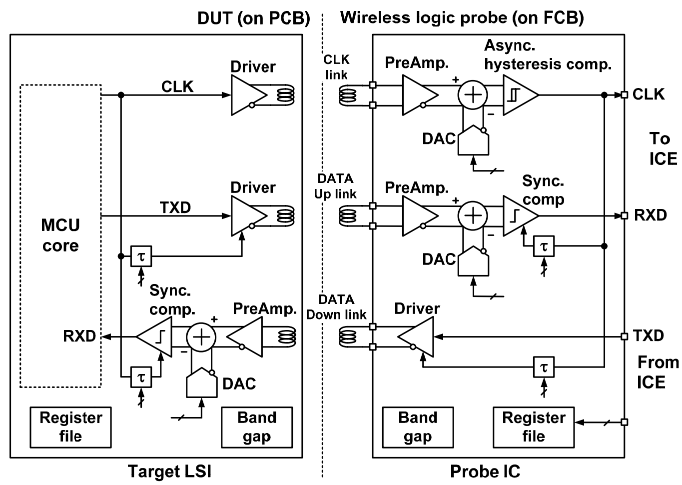

Figure 20.3.2: Transceiver block diagram.

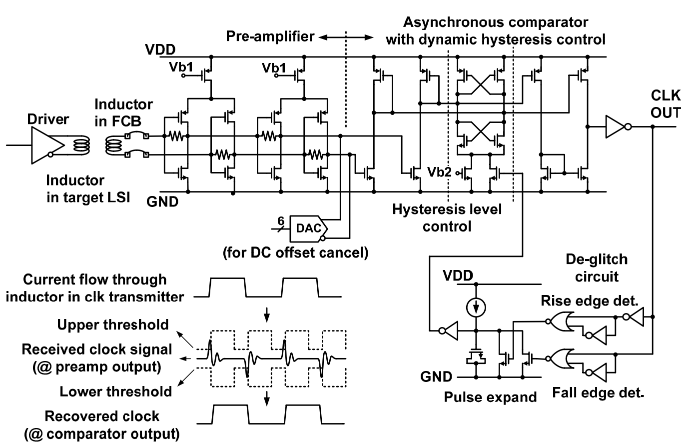

Figure 20.3.3: Clock receiver circuit.

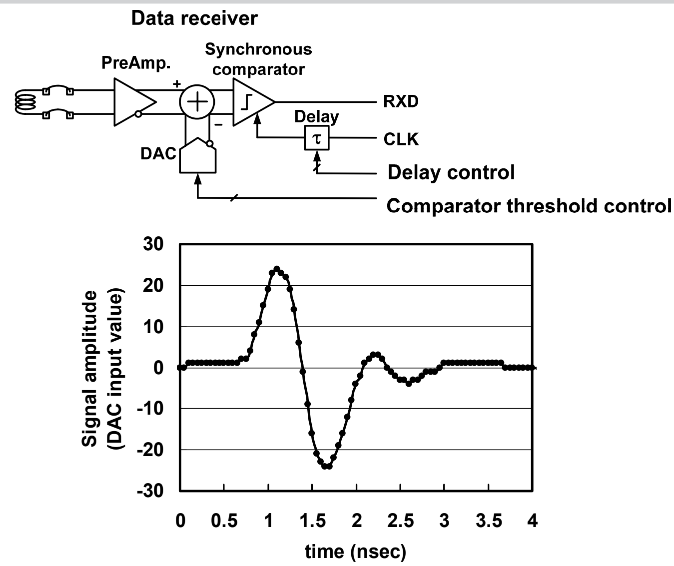

Figure 20.3.4: Measured waveform of received and amplified signal.

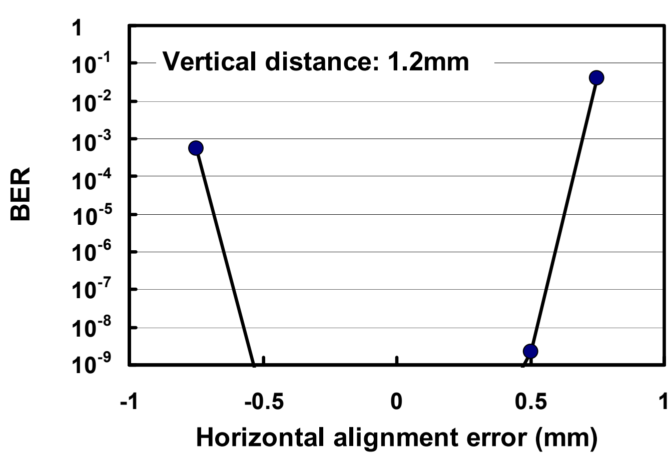

Figure 20.3.5: Measured BER dependence on horizontal alignment error.

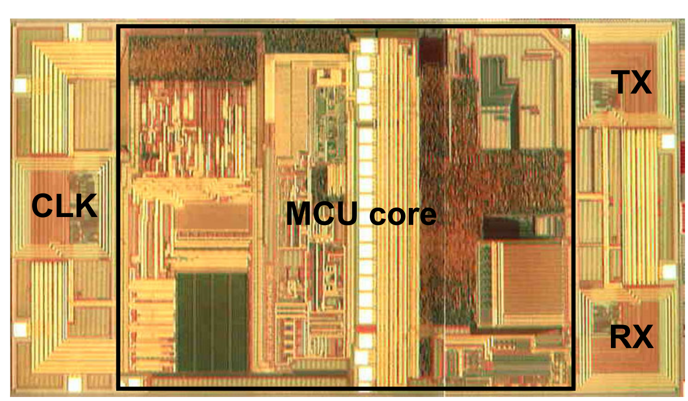

Figure 20.3.6: Die micrograph.

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Technology	0.25µm CMOS, 3-layer metal; 2-layer metal flexible circuit board
Chip size	2.4mm x 4.2mm
Supply voltage	MCU core and transceiver : 2.5V I/O : 5.0V
Data rate	20 Mb/s (full-duplex)
Communication distance	1.2mm (@ BER < 10^{-10})
Alignment tolerance	0.5mm (@ BER < 10^{-10})
Power dissipation (@20Mb/s)	CLK: TX 14.3mW, RX 10.4mW DATA: TX 0.5mW, RX 8.1mW

Figure 20.3.7: Performance summary.

